ChipEx 2024

May 7, 2024 - Expo Tel Aviv, Hall # 10				
8:00am-9:00am	**Registration and Welcome Coffee**			
08:00am	**Opening of Vendors' Exhibition**			
9:00am-11:00am	**PLENARY SESSION**			
9:00am-9:20am	**Welcome Greetings - Shlomo (Sol) Gradman**, CEO, ASG, Co-Chairman, ChipEx2024 & **Zvica Goltzman,** Deputy Head of the National Program for AI & Semiconductor Sectors, Israel Innovation Authority			
9:20am-9:40am	**The Impact of Silicon Innovation on Data Centers Performance and Efficiency**, **Adi Habusha**, Senior Principal Engineer and Chief Architect, AWS Graviton			
9:40am-10:00am	**Increasing Productivity in VLSI Using Machine Learning**, **Dalia Karmon Haim**, Director, Silicon Engineering Group, Apple Israel			
10:00am-10:20am	**EDA is Shaping the Future of Quantum Computing Software, Nir Minerbi**, Co-Founder & CEO, Classiq Quantum Computing			
10:20am-10:40am	**Re-Igniting Israel Semi Startup Scene**, **Avi Tel-Or**, CTO, Intel Ignite TLV			
10:40am-11:00am	**Introducing the Indian Delegation Companies at ChipEx2024**			
11:00am-12:00pm	**Coffee Break & Visiting the Vendors' Exhibition**			
12:00pm-1:00pm	**TECHNICAL SESSIONS - ROUND 1**			
TRACK	**Track A**	**Track B**	**Track C**	**Track D**
Track Topic	**What's Next in Chip Design**	**Power Management & Memory Design**	**ASIC IPs & FPGA**	**Chip Design, Verification & Validation**
Moderator	**Dr. Roni El-Bahar,** CTO & Co-Founder, Retym	**Prof. Alex Fish,** Bar Ilan University	**Yuri Miroshnik,** Director, IC Design Engineering, Broadcom	**Andy Carmon,** Technical Program Manager, Intel
12:00pm-12:20pm	**Leveraging Nextgen Storage Technologies for Extreme Performance and Low Latency**, **Barak Epstein**, Product Manager, Cloud HPC Storage, Google, New York	**5nm Embedded Cache Design- Challenges and Innovation**, **Noam Jungmann**, Senior Technical Staff Member, IBM	**AI inferencing and computer vision acceleration using a vector DSP**, **Ohad Ashkenazi**, Computer Vision Senior Group Leader, CEVA	**Veloce CS the Full HW Solution for Validation and Verification**, **Ohad Havshush**, Emulation Product Engineer, Siemens
12:20pm-12:40pm	**Accelerating Runtime Without Changing EDA Flows Using AWS Compute Options**, **Hannah Karlsbrun**, Sr. Solutions Architect, Amazon Web Services	**CXL Smart Memory Controller and The Importance of RAS at Data Centers**, **Yaron Bar Sinai**, Israel Site Manager, Astera Labs	**From the Cloud to Edge - FPGA Breakthrough Technologies**, **Ilan Hochman**, Israel Sales Manager, Altera	**VerifyGPT: The Path Towards This Reality**, **David Kelf**, CEO, Breker Verification Systems
12:40pm-1:00pm	**Silicon Solutions for The Next Digital Generation**, **Satish Premanatha**n, VP Engineering, HCLTech	**Power Management trends, applications and technological solutions**, **Erez Sarig**, Director of Business Development & Marketing, Tower Semiconductor	TBD	**Methodology Pioneering Automation in Verification of Processor Microarchitecture**, **Gerardo Nahum**, Sr. Application Engineer for Formal Verification, Siemens
1:00pm-2:30pm	**Lunch Break & Visiting the Vendors' Exhibition**			
2:30pm-3:30pm	**TECHNICAL SESSIONS - ROUND 2**			
TRACK	**Track E**	**Track F**	**Track G**	**Track H**
Track Topic	**Optimized Power Design**	**Designing with the Power of AI**	**Packaging and Chiplets**	**Testing, Security and Safety**
Moderator	**Zvika Bronstein,** Manager Corp. Development, Huawei	**Dror Avni,** Industry Expert	**Amnon Peled,** Consultant for Semiconductor (IC) Production	**Zmira Lavie Shterenfeld,** Partner, M&T Semiconductor
2:30pm-2:50pm	**Detection and Active Mitigation of Voltage Droop, Scott Howe**, Senior Director of Customer Success, Movellus	**Breakthrough AI accelerators and Vision Processors for Embedded Deep Learning Applications**, **Orr Danon**, CEO, Hailo	**3DIC Physical Implementation and 3D Chiplets Silicon Testing Results**, **Igor Elkanovich**, CTO, GUC	**Making It Work Right, The First Time**, **Oren Hemo**, Engineering Manager, Teradyne Israel
2:50pm-3:10pm	**Application-Specific Power Reduction Based on Chip Telemetry**, **Inbar Weintrob**, VP Silicon Technologies, ProteanTecs	**Tessent Using AI to Improve Customer DFT Results**, **Shani Eliyahu,** DFT Application Engineer, Siemens	**Unlocking the Potential of Silicon Photonics in 3DICs Addressing Multi-Physics Chalenges**, **Jerome Toublanc**, Product Manager, High-Tech Solutions, ANSYS	**Accelerated Computing Platform Security Architecture**, **Dotan Finkelshtein**, Director of Cyber Security Architecture, NVIDIA
3:10pm-3:30pm	**Tailor-Made for Efficiency: Innovating an Ultra-Low Power Implementation Flow**, **Ron Blum**, ASIC Project Lead, Avnet Asic Israel	**Extremely Low Power Micro Architectures for AI Accelerators, Tuvia Liran**, Research Fellow, Ramon.Space	**Microelectronic Packaging - From the Need to the End**, **Aviv Ronen**, Chief Technology Officer, Beckermus Technologies	**Converging on ISO-26262 ASIL-B metrics for Vision AI DSP IP using STL**, **Ayman Mouallem**, R&D Manager, Optima Design Automation
3:30pm-4:30pm	**Happy Hour**			
4:30pm-4:40pm	**Lucky Draw of the ChipEx2024 Big Prize**			
5:00pm	**END OF CHIPEX2024 DAY EVENT**			

*Program is subject to changes without notice